Boston, MA

+1 401 477 4763
chris@pacejo.net

Christopher Pacejo

Experienced network and storage systems programmer and distributed systems architect with a strong background in formal techniques.

I am a…

- detail-oriented engineer, attentive to the big picture
- creative architect, attentive to the practical
- believer in robust and accessible system design
- student of both theory and practice

My employers ask me to…

- lead groups in design and specification of new systems
- empower peers by giving accessible and informative presentations on complex topics
- evaluate, and propose and implement solutions to, system-wide architectural issues
- eliminate complexity from and improve reliability of problematic codebases
- acquire and institutionalize deep knowledge of unfamiliar codebases
- provide technical guidance for critical decisions

My peers seek my help with…

- designing and evaluating concurrent algorithms
- understanding idiomatic, correct, and performant use of modern C++
- resolving semantic mismatches at the root of architectural issues
- understanding unfamiliar systems and languages
- eliminating performance bottlenecks in both CPU-bound and I/O-bound code paths
- building robust and reliable core infrastructure

Ask me to share more about…

- proving correctness of distributed algorithms running on eventually consistent storage
- reworking an inefficient offline algorithm as an efficient online one, guided by formal methods tools
- analyzing linear checksums for strength, orthogonality, and uniformity
- developing competitive AIs to play my two favorite board games

Experience

2018–present **NuoDB** (Cambridge, MA)
Software Engineer, indexing team

- developed formal verification framework for distributed object replication protocol in TLA$^+$
- applied automatic theorem solver (Z3) to discover bugs in code refactor
- developed and formally verified online algorithm to reduce arbitrarily large histograms with logarithmic memory overhead
- advised redesign of networking subsystem to minimize latency and stalls
- took on responsibility for orphaned feature (distributed statistics collection), delivering several solutions to ease immediate customer pain points

Specialties

Languages: C++; C; Python; OCaml; Prolog; assembly; SQL; domain-specific language (DSL) design

Formal verification: TLA$^+$/PlusCal; SMT; Z3; Coq

Systems programming: GNU/Linux; concurrency/multithreading; inter-process communication; queueing; scheduling; network processing; optimization

2014–2018 **ClearSky Data** (Boston, MA)
Consulting Engineer (2018–)
Principal Software Engineer (2014–2018)

- designed and formally verified distributed algorithm to transfer ownership of portions of petabyte-scale copy-on-write data structure
- designed, implemented, and formally verified system for fail-safe non-disruptive cross-datacenter migration of data path services
- applied formal verification to discover bugs and verify fixes in data path interaction with eventually consistent storage
- designed and implemented failover mechanism for highly-available and robust NFS & SMB frontend appliance
- designed and implemented system for non-disruptive asynchronous upgrade of data path services
- architected non-disruptive migration path between highly-available synchronously-replicated relational database services
- provided technical expertise in the use of PostgreSQL, HTTP, TCP, X.509/TLS, Pacemaker, and POSIX/Linux networking and block APIs
- gave technical talks on PostgreSQL, REST, TLA$^+$, and several internal topics

2014 **EMC/XtremIO** (Hopkinton, MA)
Senior Software Engineer

- designed networking strategy for asynchronous data replication protocol
- developed protocol for configuration synchronization within replicating pair

2011–2014 **Corero Network Security** (Hudson, MA)
Software Engineer

- designed and implemented system to generate inter-process communication layer and resource assignments for multicore processor from interface definitions (US Patent 9,442,782)
- developed 40 Gbps network packet classifier and queueing system
- designed and implemented 20 Gbps packet capture and indexing application
- developed instruction scheduler for VLIW processor

2009–2010 **Brown University** (Providence, RI)
Research Assistant, Computer Science department

- co-taught graduate course on reduction semantics

Education

2008–2010 **Brown University** (Providence, RI)
Ph. D. candidate, Computer Science

2002–2008 **Worcester Polytechnic Institute** (Worcester, MA)
M. S., Computer Science (2008)
B. S., Electrical & Computer Engineering (2006)

Distributed systems: distributed algorithm design; eventual consistency

Storage: replication; write-ahead logging (WAL); block/SAN; object/cloud

Networking: Ethernet; IPv4; IPv6; TCP; HTTP; REST; XML

Security: X.509 PKI; SSL/TLS; OpenSSL

Databases: PostgreSQL; schema design; indexing